

Course Syllabus: EET 2035C – Electrical Circuits – CRN 15832 **REV. 10**

(3 Credit Hours)

**Professor’s Information:**

**Instructor:** Dr. V. Rajaravivarma  
**Office:** West Campus, Bldg. 9 – Room 118  
**Phones:** 407-582-5739  
**Email:** [vrajaravivarma@valenciacollege.edu](mailto:vrajaravivarma@valenciacollege.edu)  
**Office Hours:** Bldg. 9 – Room 118: Monday 1:30 – 2:30 PM  
 Monday 4:30 – 5:30 PM  
 Tuesday 1:30 – 2:30 PM  
 Tuesday 4:30 – 5:30 PM  
 E-mail/Canvas message: Wednesday 8:00 – 11:00 AM  
 Thursday 8:00 – 11:00 AM  
 Friday 8:00 - 10:00 AM  
 Phone/video call/Office 9-118 in person: **by appointment**

**Class Time and Location:**

**Note:** This course is delivered in a mixed-mode format that blends on-campus and online format instruction.

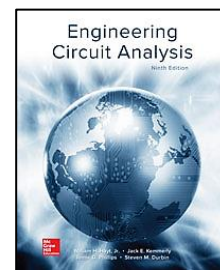
**You are required to attend class every MONDAY during the term. 2:30– 4:30 PM (Lecture & Lab: 11 – 244)**

**Course Description:**

This course introduces students to the principles and techniques required to analyze electrical circuits. Students will gain an in-depth understanding and hands-on experience with circuit simulator and laboratory projects. (Special Fee: \$82.00)

**Pre-requisites:** EET 1214C and MAC 1140 or department approval

**Textbook:** *Engineering Circuit Analysis, 9<sup>th</sup> Edition*, by William Hayt, Jack Kemmerly, and Steven Durbin; ISBN: 978-0-07-354551-6; Publisher: McGraw Hill



**Lab Manual:** Posted on Canvas

**Library Resources:** Dedicated Library resources (BSECET) at [Library BSECET Resources](#)

**Student Performance Assessment:**

**Grade Scales**

Pre-Labs, Laboratory Experiments, & Reports.....	30%	A	90 – 100 %
Quizzes* .....	15%	B	80 – 89 %
Two Exams* (15% each) .....	30%	C	70 – 79 %
Final (Theory & Lab) Exam ( <b>Comprehensive</b> ) .....	25%	D	60 – 69 %
*No make-up quizzes and exams will be given.		F	< 59 %

**Important Dates:**

Drop/Refund Deadline	August 28 <sup>th</sup>
No Show Reporting Period	August 30 <sup>th</sup> – September 8 <sup>th</sup>
Labor Day	September 4 <sup>th</sup>
Veterans Day	November 10 <sup>th</sup>
<b>Student-Initiated Withdrawal Deadline (“W” Grade)</b>	<b>October 27<sup>th</sup></b>
Thanksgiving Break	November 22 <sup>nd</sup> – November 26 <sup>th</sup>
Final Exam	December 4 <sup>th</sup> Monday @ 2:30 PM
Final Grades Viewable in Atlas	December 12 <sup>th</sup>

<b>Course Learning Outcomes</b>		<b>Performance Indicators – Students Will</b>
<b>A</b>	Demonstrate an understanding of basic electrical quantities (1, 3, 4)	<ol style="list-style-type: none"> <li>1. Show an understanding of voltage, current, and electrical power through numerical calculations</li> <li>2. Show conservation of power in an electrical circuit</li> </ol>
<b>B</b>	Demonstrate an understanding of basic principles of circuit analysis (1, 3, 4)	<ol style="list-style-type: none"> <li>1. Show an understanding of Ohm’s law, Kirchhoff’s Voltage Law (KVL), and Kirchhoff’s Current Law (KCL) through circuit analysis applications</li> <li>2. Show how to calculate equivalent resistance from series and parallel combination of resistors</li> <li>3. Show an understanding of voltage and current division rules</li> <li>4. Show an understanding of dependent sources and their use in circuits</li> </ol>
<b>C</b>	Analyze circuits using Mesh Current and Node Voltage Techniques (1, 3, 4)	<ol style="list-style-type: none"> <li>1. Solve circuits using mesh current and node voltage methods</li> <li>2. Be able to identify circuits with supernodes and supermeshes and apply appropriate techniques to analyze them</li> <li>3. Demonstrate the judgment as which analysis technique will be optimal for different circuits</li> </ol>
<b>D</b>	Analyze circuits using advanced analysis techniques (1, 3, 4)	<ol style="list-style-type: none"> <li>1. Analyze circuits using superposition technique</li> <li>2. Analyze circuits using Thevenin and Norton equivalent circuit techniques</li> <li>3. Be able to use maximum power transfer concept in the analysis of circuits</li> </ol>
<b>E</b>	Analyze AC sinusoidal circuits (1, 3, 4)	<ol style="list-style-type: none"> <li>1. Be able to transform a time-domain sinusoidal circuit into frequency (phasor) domain and vice-versa</li> <li>2. Use circuit analysis rules and techniques learned so far to analyze AC sinusoidal circuits</li> </ol>
<b>Relationship of Course’s Student Learning Outcomes to Valencia College B.S.E.C.E.T. Program Student Outcomes (ABET-ETAC)</b>		
<b>(1)</b>	An ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly-defined engineering problems appropriate to the discipline;	
<b>(2)</b>	An ability to design systems, components, or processes meeting specified needs for broadly-defined engineering problems appropriate to the discipline;	
<b>(3)</b>	An ability to apply written, oral, and graphical communication in broadly-defined technical and non-technical environments; and an ability to identify and use appropriate technical literature;	
<b>(4)</b>	An ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results to improve processes; and	
<b>(5)</b>	An ability to function effectively as a member as well as a leader on technical teams.	

### Course Learning Outcomes & Performance Indicators:

**Course Learning Outcomes** indicate the knowledge that a student should gain in this course.★

**Performance Indicators** represent how that knowledge is measured.

★ Numbers in parenthesis refer to the most recent (1) through (5) student outcome criteria of the Accreditation Board for Engineering and Technology (ABET-ETAC) met by the corresponding course student outcomes/objective(s). The ABET student outcome criteria are listed under the Valencia College B.S.E.C.E.T. Program Student Outcomes of this syllabus.

## Major Topics Covered and schedule:

Topics	# of Weeks
Basic Components and Electric Circuits, Kirchhoff's Law, Energy, and Power	1.5
Series, Parallel, and Series-Parallel Circuits	2.5
Nodal and Mesh Analysis	2.5
Source Transformation, Superposition principle, Thévenin and Norton equivalents	2.5
Energy storing elements; capacitors and inductors	1
Sinusoidal analysis and Phasors	1.5
Lab Experiments	5

## Homework Assignment:

Please submit **on time** the following Chapter Homework Assignments via Class Canvas Homepage. This selection may not give you sufficient practice. Consider your own level of understanding, and practice additional problems as needed. The purpose of the homework is for you to practice the techniques discussed in class or to reinforce this material. Completion of the recommended homework is important to master this material. Collaboration and discussion of the homework is encouraged.

EET 2035C – Homework Assignment	
Chapter	Problems
2	7-8, 10, 11, 14-15, 17, 19, 20-22, 27, 30-31, 35, 37, 40-41, 47, 54, 57
3	6, 9, 11-13, 19, 21, 23, 28, 31, 40, 46, 48-49, 56, 60
4	4, 8, 12-13, 19, 22, 25, 27, 31, 36, 38, 42, 47, 50
5	7, 11-12, 18, 21, 24, 27-29, 35, 37, 40, 44, 50, 52, 54
10	1, 3, 10, 12, 14-15, 19, 24, 27-29, 34-36, 38, 41, 45, 49

## Lab (Assignments) Requirements

- A written lab report will accompany every exercise done in this course. It is the student's responsibility to submit all lab reports via Class Canvas Homepage by the **due date**.
- Every report should be typed. **NO** hand written reports (including hand-drawn tables within the body of the report or scanned materials) will be accepted.
- All labs must be done **during assigned lab** time. Labs will only be accepted if performed during the assigned class time. ***No Lab will be accepted if performed in the open lab unless prior approval by the instructor is granted.***
- **Pre-labs** should be done ***before the beginning of class*** else you will not be able to finish the lab as lab calculations come from pre-labs. In addition, if you do any pre-lab work after lab has started, you will not receive any points for that pre-lab.
- No Late report is accepted.

***Must be ready to perform the required laboratory exercises upon arrival to the lab.***

## Note

- Even though most of the course material is covered in the textbook, the lectures may or may not necessarily follow the text word-by-word. Therefore, it is the student's responsibility to be in class and take notes. Exams will cover all material covered in class and recommended homework.
- ***This course is about your ability to excel and improve your aptitude to correctly and properly think, analyze, process, and solve circuit analysis problems as a future engineer.***

## Rules and Comments

- You are expected to be in class on time and prepared to take notes of any information and/or assignments given during class.
- **Absolutely no food or drinks** are allowed in the laboratories.
- **Exams and Quizzes:**
  - Are given at the **beginning of online assigned time**. Arrive at proper time not to miss any quiz/exam.
  - No make-up quizzes or exams are given unless **prior arrangement** with the professor has been made and **approved**.
  - Your quizzes and exams must properly show detailed work and adequately organized to earn credit. Simply written down answers will not be given any credits.
  - Exams will cover all material covered in class, labs, and recommended homework.
- There are no **dropped** exam scores.
- Final exam is comprehensive. Failing to take the final exam will result in grade F.
- **More than two unexcused absences could result in withdrawal from the course or grade F.**
- It is your responsibility to withdraw from the course. Failure to do so may result in grade F.
- **You are encouraged to ask relevant questions during class.**
- If you wish to discuss your grades, please visit my office. Valencia prohibits disclosure of grades over the phone or e-mail except through your Atlas account.
- As a courtesy to the instructor and other students in the class, the use of cell phones, pagers, text messaging, personal music devices, etc. is prohibited during class and Zoom sessions. Computers are to be used only for class-related activities, such as note taking.
- **Intellectual Freedom and Viewpoint Diversity:** It is important to be respectful of your peers' rights to privacy. Students may record video or audio of class lectures for their own personal educational use. A class lecture is defined as a planned presentation by a college faculty member or instructor, during a scheduled class, delivered for the purpose of transmitting knowledge or information that is reasonably related to the pedagogical objective of the course in which the student is enrolled.

Recording class activities other than class lectures, including but not limited to class discussions, student presentations, labs, group work, academic exercises involving student participation, and private conversations, is prohibited. Recordings may not include the image or voice of other students in the class, may not be used as a substitute for class participation and class attendance, and may not be published or shared without the written consent of the faculty member. Failure to adhere to these requirements may constitute a violation of the College's Student Code of Conduct.

**Cheating & Plagiarism:** Each student is responsible for his or her own work. All exams and graded assignments are to be exclusively your own work, unless you receive instructions otherwise.

Any academic violations or misconducts using ***human, written, electronic, software, online websites, or other resources*** in any manner not explicitly authorized by the instructor is prohibited.

The professor may assign an academic sanction to the responsible student. **Academic penalties may include, without limitation**, one or more of the following: loss of credit for an assignment, examination, or project; withdrawal from course; a reduction in the course grade; or **a grade of "F" in the course**, and **recommend expulsion from the program**. For further details see

[\*\*Valencia Academic Honesty Policy & Procedures \(Policy: 6Hx28:8-11\)\*\*](#)

**Disruptive Behavior:** Any student engaging in disruptive behavior will be advised on the first offense and will be **dropped** from the course on the second offense.

Students are strongly encouraged to read Valencia College policies of [\*\*\*Student Code of Conduct\*\*\*](#) and [\*\*\*Student Core Competencies\*\*\*](#) found at the following links:

[\*\*Student Code of Conduct\*\*](#)

[\*\*Student Core Competencies\*\*](#).

### **Students with disabilities**

Students with disabilities who qualify for academic accommodations must provide a letter from the [\*\*Office for Students with Disabilities \(OSD\)\*\*](#) and discuss specific needs with the professor, preferably during the first two weeks of class. The Office for Students with Disabilities determines accommodations based on appropriate documentation of disabilities. OSD office at West Campus is located at

Student Services Building (SSB), Room 102, Phone: 407-582-1523, Fax: 407-582-1326

Email: [\*\*osdwest@valenciacollege.edu\*\*](mailto:osdwest@valenciacollege.edu)

### **Mask policy and CDC Physical Distancing Guidelines**

The health and safety of everyone at the college is our top priority. Therefore, anyone attending the class is expected to wear masks indoors and maintain physical distancing. If you do not have a mask, the college will provide one for you. You may find it helpful to refer to current research on the importance of masking for public safety. Feel free to check out the CDC guidelines on masking, [\*\*located at this link\*\*](#).

### **COVID-19 Wellness, Reporting, and Support**

If you find yourself feeling unwell and suspect you might be experiencing symptoms of COVID-19, test positive for COVID-19, or have been in close contact with someone who has the COVID-19 virus, please stay home. Please also report this to Valencia's COVID-19 case manager Tanya Mahan, at [\*\*COVIDillness@valenciacollege.edu\*\*](mailto:COVIDillness@valenciacollege.edu), so the College can determine how to best support you.

If you are unable to participate in the course due to illness, family emergency, etc., please communicate with me as soon as possible in order to create a plan for the best course of action. In the case of a prolonged online absence of one week or more, you and I will meet to discuss options and determine your ability to continue in the course.

### **Monitoring COVID-19**

- Find information and a list of resources on what you need to know about the coronavirus at [\*\*https://valenciacollege.edu/alerts/covid-19.php\*\*](https://valenciacollege.edu/alerts/covid-19.php)
- [\*\*https://valenciacollege.edu/about/coronavirus/documents/rtr-illness-reporting.pdf\*\*](https://valenciacollege.edu/about/coronavirus/documents/rtr-illness-reporting.pdf)
- [\*\*https://www.cdc.gov/coronavirus/2019-ncov/downloads/sick-with-2019-nCoV-fact-sheet.pdf\*\*](https://www.cdc.gov/coronavirus/2019-ncov/downloads/sick-with-2019-nCoV-fact-sheet.pdf)
- [\*\*https://floridahealthcovid19.gov/treatment/\*\*](https://floridahealthcovid19.gov/treatment/)
- [\*\*https://uwcf.org/covid19-resources/\*\*](https://uwcf.org/covid19-resources/)

**Tentative Course Outline for EET 2035C – CRN 15832; Fall 2023**

**Submit all weekly assessments via Canvas by Saturday Midnight**

Week	Dates	Topics	Chapter
1	21–Aug.	Introduction; Engineering prefixes; Charge, current, voltage, and power; Independent & Dependent sources; Resistors	2
2	28–Aug.	Resistance combination; Ohm’s Law; Power absorption; Conductance Nodes, paths, loops, and branches; KVL, KCL, and Single Loop circuit	2 3
3	4–Sept.	<b>Labor Day – No Class Monday – College Closed</b>	
		Series & parallel resistance, Voltage & Current division, Series & parallel Circuits	3
4	11–Sept.	<b>Lab 1 – Current, Voltage and Resistance in Series and Parallel Circuits</b> (REPORT DUE – Saturday midnight, September 16)	<b>DUE</b>
		Series & parallel Circuits – <i>Continued...</i> <b>Quiz 1 – Chapter 2</b>	3
5	18–Sept.	<b>Lab 2 – Series and Parallel Combination Circuits</b> <b>Quiz 2 – Chapter 3</b> (REPORT DUE – Saturday midnight , September 23)	<b>DUE</b>
6	25–Sept.	<b>Exam 1 – Chapters 2 &amp; 3 (Monday, September 25)</b>	
		Nodal Analysis and Supernodes	4
7	2–Oct.	Nodal Analysis and Supernodes – <i>Continued...</i> Mesh Analysis and Supermesh <b>Quiz 3 – Chapter 4 (Node Analysis)</b>	4
8	9–Oct.	Mesh Analysis and Supermesh – <i>Continued...</i> <b>Quiz 4 – Chapter 4 (Mesh Analysis)</b>	4
9	16–Oct.	<b>Lab 3 – Node, Mesh, Linearity, and Superposition Theorems</b> (REPORT DUE – Saturday midnight , October 21)	<b>DUE</b>
		Linearity; Superposition & Source Transformation	5
10	23–Oct.	Thévenin Equivalent Circuits ( <b>TEC</b> ) <b>Quiz 5 – Chapter 5 (Superposition)</b> <b>Quiz 6 – Chapter 5 (Source transformation)</b>	5
11	30–Oct.	<b>Lab 4 – Proof of Thévenin, Norton and Maximum Power Transfer Theorems</b> (REPORT DUE – Saturday midnight , November 4)	<b>DUE</b>
		<b>TEC</b> – <i>Continued...</i> and Norton Equivalent Circuits ( <b>NEC</b> )	5
12	6–Nov.	<b>TEC / NEC</b> and Maximum power transfer – <i>Continued...</i> <b>Quiz 7 – Chapter 5 (TEC)</b>	5

13	13–Nov.	<b>Exam 2 – Chapters 4 &amp; 5, and Labs 2 – 4 (Monday, November 13)</b>	
		Complex Numbers, Rectangular and Polar Coordinate systems and conversions <i>(Instructor provided materials/notes on Course Canvas Page)</i>	<b>Notes</b>
14	20–Nov.	Sinusoidal signals; Phasors and Phasor Diagrams; Impedance and conversion from time to phasor domain <b>Quiz 8 – (Complex Numbers/Rectangular/Polar Coordinate Systems)</b>	<b>Notes</b>
15	27–Nov.	<b>Lab 5 – AC Sinusoidal Circuits</b> <b>(REPORT DUE – Saturday midnight , December 2)</b>	<b>DUE</b>
16	<b>Dec. 4</b>	<b>Final Exam (Theory &amp; Lab) – Comprehensive – Monday, Dec. 4 at 2:30 PM</b>	